Remarks

Claims 1-11 and 14-20 are pending. Claims 12 and 13 have been cancelled. Claims 9 and 14 have been amended.

In the Specification

The specification has been amended as illustrated above to correct several typographical errors. No new matter has been added.

In the Drawings

The drawings are objected to because the reference character **23** has been used to designate both a buffer and a register in **Figure 2**. **Figure 2** has been amended to correct this error as shown in the attached appendix. No new matter has been added.

Rejection of Claims under 35 U.S.C. § 112

Claim 1 is rejected under 35 U.S.C. § 112, first paragraph, as based on disclosure that is not enabling. The applicant respectfully traverses this rejection.

In making this rejection, the Examiner appears to make use of form paragraph 7.31.01 (MPEP § 706.03(c)). In following the form paragraph and the MPEP's accompanying instructions, the Examiner's identifies as an aspect of the claim for which the specification is not enabling that "the destination transmit clock domain with first and second input, but with *only* the first input being coupled to the source transmit clock domain." Office Action of April 9, 2003, p. 2, no. 3, emphasis added. In explaining why the specification is not enabling, the Examiner states:

> The specification enable for a destination transmit clock domain with two inputs, both coupled to the source transmit clock domain. However, the specification does not enable for a destination transmit clock domain with two input signals, but only one input is coupled to the source transmit clock domain as recite in claim 1 lines 10-13.

The applicant respectfully disagrees. In enabling a circuit with a destination clock domain having a register including a first and a second input, e.g., domain **5** and register **21**, and in enabling such a circuit where both the first input and the second input are coupled to respective signal sources in a source clock domain, e.g., signals **8** and **10**, the applicant has necessarily enabled an open claim (e.g., wherein the preamble indicates that

it *comprises* one or more elements) where one of the first and second inputs is coupled to the source clock domain. The applicant further notes that the Examiner appears to suggest that claim 1 requires that "*only* the first input being coupled to the source transmit clock domain." There is no such requirement in the claim.

Additionally, the applicant respectfully submits that there is sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention without undue or unreasonable experimentation. In order to satisfy the enablement requirement of 35 USC § 112, the disclosure must have sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention without undue or unreasonable experimentation. Regarding the level of skill of one having ordinary skill in the art, "the examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made." MPEP § 2142. The courts have provided even clearer guidelines regarding a person of ordinary skill:

> The person of ordinary skill is a hypothetical person who is presumed to be aware of all the pertinent prior art. The actual inventor's skill is not determinative. Factors that may be considered in determining level of skill include: type of problems encountered in art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field. Not all such factors may be present in every case, and one or more of them may predominate. *Custom Accessories, Inc. v. Jeffrey-Allan Indus., Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986).

Thus, if the Examiner asserts that the disclosure does not have sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention without undue or unreasonable experimentation, he must demonstrate this in accordance with MPEP § 2164. Contrary to the suggestion of Examiner Note 6 accompanying form paragraph 7.31.03, the Examiner has not so demonstrated.

Accordingly, the applicant respectfully submits that claim 1 is enabled and therefore allowable.

Claims 9 and 14 are rejected under 35 U.S.C. § 112, second paragraph because the Examiner asserts that the term "sourcing" is unclear. The applicant notes that the term as used in claims 9 and 14 is well understood to those having ordinary skill in the art and further that use of the term finds support in the specification on, for example, page 5. Nevertheless, and in the interest of advancing prosecution of this application, claims 9 and 14 have been amended to address this rejection.

Accordingly, the applicant respectfully submits that claims 9 and 14 are definite and therefore allowable.

Rejection of Claims under 35 U.S.C. § 102/103

Claims 1-4, 6, 7, and 9-19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Ishikawa, U.S. Patent No. 5,748,018. Claims 5, 8, and 20 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Ishikawa in view of Nichols et al., U.S. Patent No. 6,356,557 B1 (Nichols). The applicant respectfully traverses these rejections.

Ishikawa neither teaches nor suggests a source clock domain in a first layer including:

> a buffer having an input for receiving the clock signal and an output, said buffer generating a delay that is substantially equivalent to a delay through said register,

as required by independent claim 1. The applicant notes that regarding the claimed "source clock domain *in a first layer*," the Examiner points to nothing in Ishikawa teaching or suggesting this limitation. Regarding the claimed buffer generating a delay that is substantially equivalent to a delay through said register, the Examiner refers to column 4, lines 29-33 of Ishikawa. The relevant portions of Ishikawa (including that portion cited by the Examiner) state:

> Referring to FIG. 2B, there is shown a timing chart illustrating an operation of the data output circuit shown in FIG. 2A. In addition, assuming that an internal delay time of the D-FF **101** as compared with the external clock signal CLK is t_q, and a delay time of the output buffer **102** as compared with the output of the D-FF **101** is t_b, a delay time t_d in the data transfer as compared with the external clock CLK is expressed as $t_q + t_b$. On the other hand, assuming that a difference in time between the

> external clock signal CLK and the delayed clock signal CLKD is t_b, a delay time t_D in the data transfer as compared with the delayed clock CLKD is expressed as follows:
>
> $t_D = t_q + t_b - t_b = t_q$
>
> Accordingly, the delay time t_D in the data transfer becomes equal to t_q, and therefore, this becomes substantially equivalent to the fact that the internal clock signal is advanced as compared with the external clock by the time t_b by using the PLL circuit.

Thus, nothing in the referenced portion of Ishikawa teaches or suggests that the delay t_b generated by buffer **103** (i.e., that which the Examiner contends teaches the applicant's claimed buffer) is substantially equivalent to a delay through flip flop **101** (i.e., that which the Examiner contends teaches the applicant's claimed source clock domain register). In other words, there is nothing in the cited portion of Ishikawa teaching or suggesting that t_b is substantially equivalent to t_q.

Accordingly, the applicant respectfully submits that claim 1 is allowable over Ishikawa. Claims 2-8 depend from claim 1 and are allowable for at least this reason.

Ishikawa neither teaches nor suggests a method including:

> sending the clock input through a buffer, the buffer having a delay which is equal to the delay through the latching device,

as required by independent claim 14 and generally required by independent claim 9 as amended.

Regarding the claimed feature that the buffer has a delay which is equal to the delay through the latching device, the Examiner refers to column 4, lines 10-14 of Ishikawa. The relevant portion of Ishikawa (including that portion cited by the Examiner) states:

> As shown in FIG. 2A, a data output circuit **100** includes a D-FF D-type flipflop) **101** having a data input "D" receiving data to be transferred and a clock input "CK" connected to a clock terminal **104** to receive a clock signal CLK supplied from an external device (not shown), and an output buffer **102** having an input connected to a non-inverted data output Q of the D-FF **101** and an output connected to a data output terminal **106** for outputting the data, and another output buffer **103** having an input connected to the clock terminal **104** to receive the external clock CLK and an output connected to a clock output terminal **105** for outputting a

delayed clock CLKD which is delayed from the external clock signal CLK by a delay time of the output buffer **103**.

Thus, nothing in either this referenced portion of Ishikawa or the portions quoted above teaches or suggests that buffer **103** (i.e., that which the Examiner contends teaches the applicant's claimed buffer) has a delay which is equal to the delay through flip flop **101** (i.e., that which the Examiner contends teaches the applicant's claimed latching device). In other words, there is nothing in the cited portion of Ishikawa teaching or suggesting that t_b is equivalent to t_q.

Accordingly, the applicant respectfully submits that claims 9 and 14 are allowable over Ishikawa. Claims 10 and 11 depend from claim 9 and are allowable for at least this reason. Claims 15-20 depend from claim 14 and are allowable for at least this reason.

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the examiner is requested to telephone the undersigned.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop: Non fee Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA, 22313-1450, on July 9, 2003.

Attorney for Applicant(s) — Date of Signature: 7/9/03

Respectfully submitted,

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ANNOTATED SHEET SHOWING CHANGES

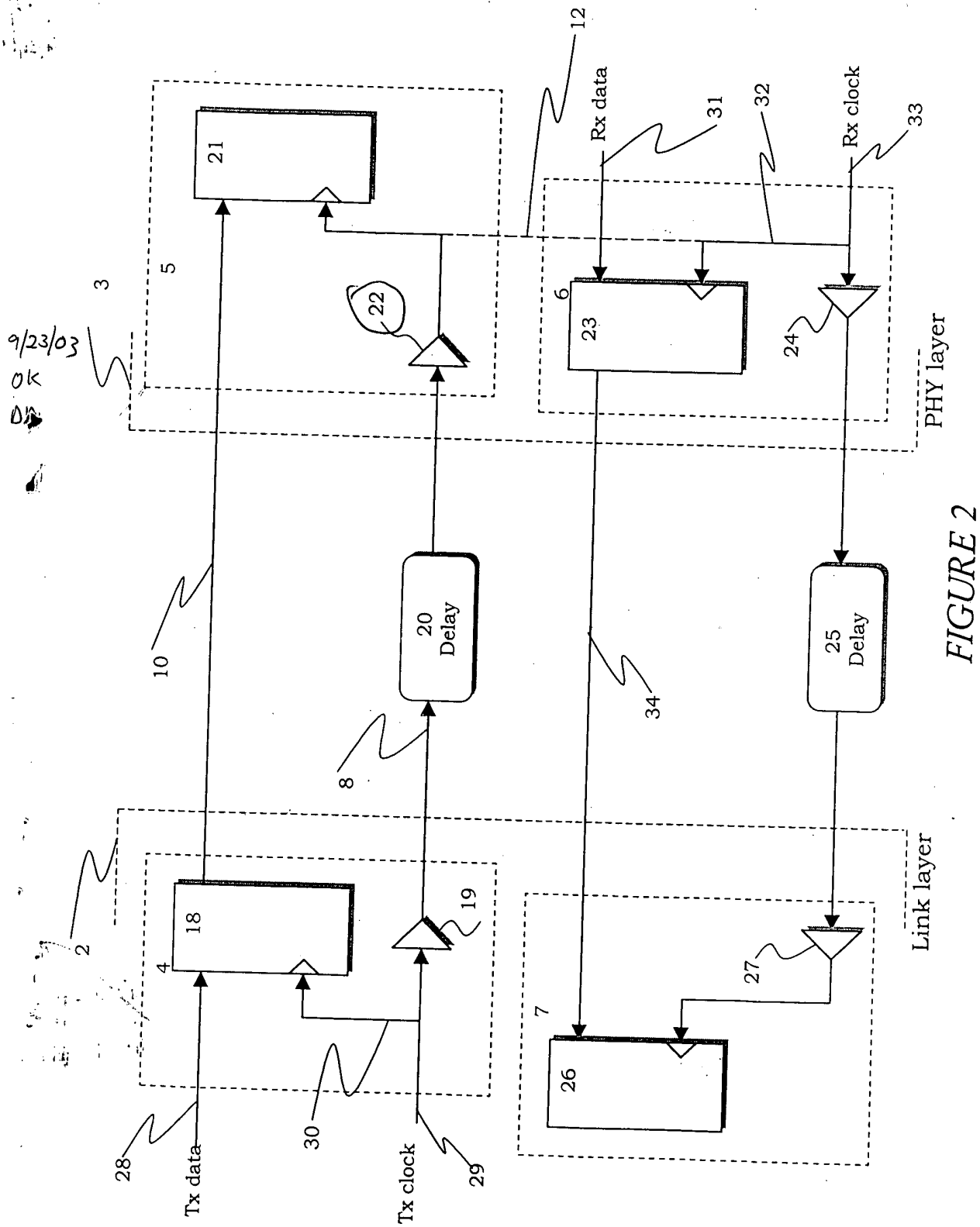

FIGURE 2